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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,017	02/09/2004	Makoto Fujiwara	790001-2043	9801

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EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,017	FUJIWARA ET AL.	
	Examiner	Art Unit	
	Ida M. Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *20-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-8,11,13-16,18 and 19* is/are rejected.

7)☒ Claim(s) *4,9,10,12 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2-9-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the election filed May 2, 2005.

Election/Restrictions

Applicant's election without traverse of claims 1-19 in the reply filed on May 2, 2005 is acknowledged.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 16 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is not understood how an insulating layer formed between the silicide layer on the upper portion of the semiconductor layer and the semiconductor layer.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3 and 5-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Inaba et al. (US 6,525,403 B2).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In regard to claim 1, Inaba et al. teach semiconductor device comprising: a semiconductor substrate 11; a fin-shaped semiconductor layer 11A which is formed on the semiconductor substrate 11, is long in a first direction and is short in a second direction crossing the first direction; a gate insulating layer 13 formed on side surfaces of the semiconductor layer 11A in the second direction; gate electrode 14 arranged so as be adjacent the gate insulating layer 13; channel area formed at a position adjacent to the gate insulating layer 13 in the semiconductor layer 11A; a source/drain extension

area which is formed at a position adjacent to the channel area in the semiconductor layer in the first direction; and a source/drain area 15/16 which is formed at a position adjacent to the source/drain extension area in the semiconductor layer 11A in the first direction, wherein a width of the semiconductor layer 11A in the channel area (the width under gate electrode 14 See Figure 11A) in the second direction is smaller than a width of the semiconductor layer 11A in the source/drain area 15/16 in the second direction (Figures 7 and 11A, columns 4-5, lines 16-67 and 1-11, respectively).

In regard to claim 2, Inaba et al. teach the width of the semiconductor layer 11A in the channel area in the second direction is smaller than a width of the semiconductor layer in the source/drain extension area (the area that angles toward gate 14 in Figure 11A) in the second direction (Figures 7 and 11A, columns 4-5, lines 16-67 and 1-11, respectively).

In regard to claim 3, Inaba et al. teach the width of the semiconductor layer 11A in the source/drain extension area (the area that angles toward gate 14 in Figure 11A) in the second direction is smaller than the width of the semiconductor layer in the source/drain area 15/16 in the second direction (Figures 7 and 11A, columns 4-5, lines 16-67 and 1-11, respectively).

In regard to claim 5, Inaba et al. teach the width of the semiconductor layer 11A in the channel area in the second direction is smaller than a gate length of the gate electrode 14 (Figures 7 and 11A, columns 4-5, lines 16-67 and 1-11, respectively).

In regard to claim 6, Inaba et al. teach the width of the semiconductor layer in the source/drain extension area (the area that angles toward gate 14 in Figure 11A) in the

second direction is equal to or larger than a gate length of the gate electrode (Figures 7 and 11A, columns 4-5, lines 16-67 and 1-11, respectively).

In regard to claim 7, Inaba et al. teach the gate electrode 14 constituted by a first part which is formed on one side of the semiconductor layer 11A in the second direction and a second part which is formed on the other side of the semiconductor layer in the second direction (Figure 7, columns 4-5, lines 16-67 and 1-11, respectively).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8, 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba et al (US 6,525,403 B2) in view of Aller et al. (US 2004/0222477 A1).

In regard to claim 8, a semiconductor substrate 11; a plurality of fin-shaped first semiconductor layers 11 A (title) which are formed on the semiconductor substrate 11, long in a first direction, short in a second direction crossing the first direction, and aligned in the second direction; a gate insulating layer 13 which formed on side surfaces of each of a plurality of the first semiconductor layers 11A in the second direction; gate electrode 14 arranged so as to be adjacent the gate insulating layer 13; a channel area (the area that extends between the source/drain areas 15/16) which is formed at a position adjacent to the gate insulating layer 13 in a plurality of the first semiconductor

layers 11A; a source/drain extension area (the area that angles toward gate 14 in Figure 11A) formed at a position adjacent to the channel area (the area that extends between the source/drain areas 15/16) in the first direction in a plurality of the first semiconductor layers 11A; and a source/drain area 15/16 formed at a position adjacent to the source/drain extension area (the area that angles toward gate 14 in Figure 11A) (Figures 7 and 11A, columns 4-5, lines 16-67 and 1-11, respectively).

However, Inaba et al. fail to teach a second semiconductor layer which connects a plurality of the first semiconductor layers with each other at end portions of a plurality of the first semiconductor layers in the first direction; and a source/drain area formed at a position adjacent to the source/drain extension area in the second semiconductor layer in the first direction.

Aller et al. teach a second semiconductor layer 4 which connects a plurality of the first semiconductor layers 21 with each other at end portions of a plurality of the first semiconductor layers 21 in the first direction; and a source/drain area 20 formed at a position adjacent to the source/drain extension area in the second semiconductor layer 4 in the first direction (Figure 1, page 1, paragraph [0009]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device structure as taught by Inaba et al. with the semiconductor device having a second semiconductor layer which connects a plurality of the first semiconductor layers with each other at end portions of a plurality of the first semiconductor layers in the first direction; and a source/drain area formed at a position adjacent to the source/drain extension area

(under 21 and above 4) in the second semiconductor layer in the first direction as taught by Aller et al. to resolve short channel effects (page 1, paragraph [0009]).

In regard to claim 11, Inaba et al. teach a width of each of a plurality of the first semiconductor layers 11A in the channel area (the area that extends between the source/drain areas 15/16) in the second direction is smaller than a width of each of a plurality of the first semiconductor layers in the source/drain extension area (the area that angles toward gate 14 in Figure 11A) in the second direction (Figures 7 and 11A, columns 4-5, lines 16-67 and 1-11, respectively).

In regard to claim 13, Inaba et al. teach the width of the first semiconductor layer 11A in the channel area (the area that extends between the source/drain areas 15/16) in the second direction is smaller than a gate length of the gate electrode 14 (Figures 7 and 11A, columns 4-5, lines 16-67 and 1-11, respectively).

Claims 14-16 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba et al (US 6,525,403 B2) in view of Paton et al. (US 2004/0061191 A1).

In regard to claim 14, Inaba et al. teach a semiconductor device comprising: a semiconductor substrate 11; a fin-shaped semiconductor layer 11A which is formed on the semiconductor substrate 11, is long in a first direction and is short in a second direction crossing the first direction; a gate insulating layer 13 formed on side surfaces of the semiconductor layer 11A in the second direction; gate electrode 14 arranged so as be adjacent the gate insulating layer 13; channel area formed at a position adjacent

to the gate insulating layer 13 in the semiconductor layer 11A; a source/drain extension area which is formed at a position adjacent to the channel area in the semiconductor layer in the first direction; and a source/drain area 15/16 which is formed at a position adjacent to the source/drain extension area in the semiconductor layer 11A in the first direction (Figures 7 and 11A, columns 4-5, lines 16-67 and 1-11, respectively).

However, Inaba et al. fail to teach a silicide layer which is formed on a surface portion of the semiconductor layer in the source/drain layer but not formed in the inner portion of the same.

Paton et al. teach a silicide layer 90/92which is formed on a surface portion of the semiconductor layer 86 in the source/drain layer 80 but not formed in the inner portion of the same (Figure 7, page 4, paragraph [0035]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device structure as taught by Inaba et al. with the semiconductor device having a silicide layer which is formed on a surface portion of the semiconductor layer in the source/drain layer but not formed in the inner portion of the same as taught by Paton et al. to increase device speed and performance (page 1, paragraph [0007]).

In regard to claim 15, Paton et al. teach the silicide layer 90/92 formed on an upper portion of the semiconductor layer 86 and a surface portion of the same in the second direction (Figure 7, page 4, paragraph [0035]).

As best understood, In regard to claim 16, Paton et al. teach an insulating layer (not shown) which functions as a stopper in silicidation is formed between the silicide layer on the upper portion of semiconductor layer and the semiconductor layer.

In regard to claim 18, Paton et al. teach a width of the semiconductor layer in the source/drain area 80 in the second direction is larger than a width of the semiconductor layer in the source/drain extension area or the channel area 82 in the second direction (Figure 7, page 4, paragraph [0035]).

In regard to claim 19, Paton et al. teach a height of the semiconductor layer in the source/drain area 80 is larger than a height of the semiconductor layer in the source/drain extension area or the channel area 82 (Figure 7, page 4, paragraph [0035]).

Allowable Subject Matter

Claims 4, 9-10, 12 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to FinFETs:

Clark et al. (US 6,849,884 B2) Fried et al. (US 2003/0178670 A1)

Hu et al. (US 6,413,802 B1) Kottantharayil et al. (US 2005/0093154 A1)

Liao et al. (US 6,888,181 B1) Mathew et al. (US 2004/0235300 A1)

Nowak et al. (US 2004/0262688 A1) Pham et al. (US 6,838,322 B2)

Yang et al. (US 2004/0203211 A1) Yeo et al. (US 2005/0023633 A1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
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